REMARKS

Claims 1-4 are pending in the application.

Claims 1-4 have been rejected.

Claims 1-4 have been amended, as set forth herein.

I. REJECTION UNDER 35 U.S.C. § 112

Claims 1-4 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The rejection is respectfully traversed.

Applicant has amended Claims 1 and 3-4. Applicant submits that these claims are now definite.

Accordingly, the Applicant respectfully requests withdrawal of the § 112 rejection of Claims 1-4.

II. REJECTION UNDER 35 U.S.C. § 102

Claims 1-4 were rejected under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art (Figure 2). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Independent Claim 1 recites a second inverted output (Qa2) of the second flip-flop (M1', M2', M3', M4') coupled to the first set input (Q4) of the first flip-flop (M1, M2, M3, M4). In distinct contrast, the prior art shown in Figure 2 does not disclose that the second inverted output (s/d of M1' and M4' of the second flip flop) is coupled to the first set input (Q4) of the first flip-

flop (M1, M2, M3, M4). Also, the prior art of Figure 2 describes stacked transistors, while Claim 1 recites the first and second flip-flops as being "without stacked transistors." For at least these two reasons, the admitted prior art (Figure 2) does not disclose each and every element recited in independent Claim 1 (and the dependent claims).[1]

Accordingly, the Applicant respectfully requests the Examiner withdraw the § 102(b) rejection of Claims 1-4.

III. REJECTION UNDER 35 U.S.C. § 103

Claims 1-2 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Murray (EP 0270191) in view of Edwards (US Patent Application Publication 2005/0156643). The rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more

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[1] In addition, US 6,166,571 to Wang describes a high frequency divider circuit for producing output signals of half the frequency of an input clock signal and including two identical circuit sections, each producing an output signal and its complement. The circuit sections are connected to each other so that the output signals of one circuit section serve as input signals to the other circuit section. Furthermore, each circuit section contains a load transistor which is controlled by one of the clock signal and the clock signal complement, and a switch transistor which is controlled by the other of the clock signal and the clock signal complement. Wang, Abstract. Wang describes stacked transistors. Wang, Figure 2.

the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142. In making a rejection, the examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), *viz.*, (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the art. In addition to these factual determinations, the examiner must also provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (*In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir 2006) (cited with approval in *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007)).

Murray describes a pulse train divider circuit comprising a first flip-flop whose Q output is connected to the D input of a second flip-flop whose output is connected to the D input of the first flip-flop. A pulse train to be divided is applied via an input directly to the clock input C of the first flip-flop and via a circuit which delays the pulse train applied to the clock input C of the flip-flop to provide a given phase relationship between the pulse trains at the two clock inputs. The circuit divides-by-two and the resulting divided pulse trains available at the various outputs have phase relationships depending on the phase relationship of the applied pulse trains

at the clock inputs. Murray, Abstract.

Edwards describes a high-speed, current-driven latch conducting a current and including an output, a SET circuit and a RESET circuit. Further, the output is variable between a first state and a second state. The SET circuit conducts the current present in the latch at the first stage such that the SET circuit is maintained close to a level required to change the output of the transistor from the first to the second level, and the RESET circuit conducts the current at the second level such that the RESET circuit is close to a level required to change the output of the transistor from the second level to the first level. Edwards, Abstract.

Thus, none of these references appear to disclose or describe flip-flops without stacked transistors or that the second inverted output (Qa2) of the second flip-flop is being coupled to the first set input (Q4) of the first flip-flop.

Furthermore, the subject matter of Claim 1 is not only novel, but is not obvious in view of Murray and Edwards.

One of the objects of the present invention is to provide a frequency divider suitable for low-voltage supply voltages and high-speed of operation. Further, power consumption is minimized. The prior art, on the other hand, shows that through a controlled inverter at an input of the frequency divider, the signal cannot be transmitted from the input of the controlled inverter to its output. Therefore, the controlled inverter at the input limits the maximum frequency. Thus, by inverting the phase of the feedback signal from the second flip-flop allows for an elimination of the inverter and contributes to an increase in the maximum frequency of input signals. Specification, par. [0008]. The prior art appears to also show at least two stacked transistors which are less suitable for relative low-voltage supply applications. Specification, par. [0004]. As additionally described in the Applicant's application, the frequency divider eliminates an inverter from the input of the flip-flops used. Specification, par. [0018]. The input of the first flip-flop is coupled to the inverted output of the second flip-flop which provides a signal substantially in anti-phase, i.e. phase shifted over 180 degrees with respect to the signal provided by the second output. Hence, a time delay of the signal generated by a further inverter

is avoided. These benefits/goals are achieved by the subject matter of Claim 1.

It is respectfully submitted that neither Murray or Edwards teaches or suggests the recited features of "without stacked transistors" and "the second inverted output of the second flip-flop being coupled to the first set input (Q4) of the first flip-flop." See, Claim 1. The prior art is simply mute on these issues since it simply deals with other issues.

Therefore, a person skilled in the art would obtain no motivation or suggestion from studying the prior art to arrive at the subject matter of the claimed invention. As a result, the subject matter of Claim 1 (and dependent Claim 2) is not obvious over the proposed Murray-Edwards combination.

Accordingly, the Applicant respectfully requests withdrawal of the § 103(s) rejection of Claims 1-2.

IV. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***rmccutcheon@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, P.C.

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Robert D. McCutcheon
Registration No. 38,717

P.O. Box 802432
Dallas, Texas 75380
(972) 628-3632 (direct dial)
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *rmccutcheon@munckcarter.com*